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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,970	03/30/2006	Tatsuo Hiramatsu	070456-0105	1749
20277 7590 01/09/2008 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, N.W. WASHINGTON, DC 20005-3096			EXAMINER GIROUX, GEORGE	
			ART UNIT 2183	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/573,970

Applicant(s)

HIRAMATSU ET AL.

Examiner

George Giroux

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) 1-22, 32 and 33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 23-31 and 34-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 19 October 2007, in response to the Office Action mailed 19 July 2007. The applicant's remarks and amendments to the claims and specification were considered, with the results that follow.
2. The objections to the claims and the rejection of claims 13-15 and 20 under 35 U.S.C. 112, second paragraph, have been withdrawn due to the amendments filed 19 October 2007.
3. Claims 1-22 have been cancelled, and replacement claims 23-43 have been added, related to the original claims preliminarily amended and intended for presentation, except for cancelled claims 32-33 (corresponding to old claims 10 and 11).

Response to Arguments

4. Applicant argues, regarding claim 23, that Abramovici does not teach wherein the outputs of a configured circuit are provided as an input to a circuit configured in accordance with the next setting data. However, Abramovici does teach wherein the page manager may include FIFO input buffers or other suitable sets of registers for storing inter-page signal values for loaded and unloaded pages (abstract) where the inter-page signal values between pages (pages in the page manager corresponding to configured circuits) are the output from one page (circuit) to the input of another.

Applicant also argues that Abramovici does not teach first and second data paths, where the second path portion passes through a memory portion, while the first path portion does not pass through the memory. However, Abramovici teaches a path through the page manager from one configured circuit to another (abstract) as described above, as well as a path which stores output and register values of one circuit (page) in the memory, then provides this information as the input to the next loaded circuit (page) (figure 4).

5. Applicant argues, regarding claim 34, that Abramovici does not teach the claimed control portion, which controls the setting portion to configure a plurality of intended circuits, so that setting data for configuring divided units each forming a part of the circuits are successively supplied along a process flow. However, Abramovici teaches wherein the page manager holds active and inactive configurations (pages) for the configured circuits, supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract) as described in the rejection.

In addition, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the setting portion circuits having a function different from each other as the first stage and the second stage of individual reconfigurable units simultaneously at a certain timing (first timing), and then the circuits as the second stage and third stage of the reconfigurable unit simultaneously at the next timing (second timing)) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 23-30 and 34-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici (US 6034538).

As per claim 23, Abramovici teaches a reconfigurable circuit allowing change in function as **[a set of reconfigurable hardware including a number of field programmable gate arrays (FPGAs) (abstract)]**, a first path transmitting an output of the reconfigurable circuit to an input of the reconfigurable circuit as **[a page configuration for a circuit which includes a feed-forward structure, where the outputs of one page loaded into the FPGAs feed the input of the next page loaded**

into the FPGAs (column 6, lines 31-44 and figure 5A) and the page manager (PAGMAN 22) is operative to route signals between loaded pages (column 5, lines 8-10)], a setting portion supplying setting data for configuring the reconfigurable circuit as [the local memory includes dedicated areas for storing configuration information (column 4, lines 13-15) which is supplied, via the page manager, to the FPGAs (column 5, lines 3-5)], a control portion controlling the setting portion such that a plurality of setting data sets are successively supplied to the reconfigurable circuit, so that an output of a circuit configured on the reconfigurable circuit according to one setting data set is supplied to an input of another circuit configured on the reconfigurable circuit with the next setting data through the first path as [the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) wherein the page manager holds active and inactive configurations (pages) for the configured circuits, supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)], an internal state holding circuit receiving an output of the reconfigurable circuit and connected to the first path as [the page manager (PAGMAN 22) includes one or more first-in-first-out (FIFO) buffers for use in controlling storage and transferring inter-page signal values (i.e. storing the output of one page, to be provided as the input to another) (column 5, lines 10-21 and figure 3)], a memory portion storing, in

a prescribed area, an output of a circuit configured on the reconfigurable circuit in accordance with one setting data as **[the FPGAs and the page manager communicate via bus 23 with the local memory 24 which holds output and register values from the FPGAs, as well as the configuration information (column 4, lines 8-19 and figure 2)]** and a second path transmitting the output of the circuit, configured on the reconfigurable circuit, stored in the prescribed area of the memory, as an input to a circuit configured on the reconfigurable circuit configured by the next setting data as **[a path which stores output and register values of one circuit (page) in the memory, then provides this information as the input to the next loaded circuit (page) (figure 4)]**.

As per claim 24, Abramovici teaches where the internal state holding circuit operates at a higher speed than the memory as **[the page manager (PAGMAN 22) includes one or more first-in-first-out (FIFO) buffers for use in controlling storage and transferring inter-page signal values (i.e. storing the output of one page, to be provided as the input to another) (column 5, lines 10-21 and figure 3), whereas the page manager must communicate with the local memory via a bus (column 4, lines 8-19) so the buffers are inherently faster than the memory access]**.

As per claim 25, Abramovici teaches wherein the setting portion successively supplies a plurality of setting data to the reconfigurable circuit so that one circuit is formed as a whole as **[the set of FPGAs which form the reconfigurable hardware**

implements a single logic circuit, having any desired size, by partitioning the circuit's netlist into "subcircuit portions", each of which is represented by a portion of the initial netlist generally referred to as a page (column 3, lines 32-45) supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)].

As per claim 26, Abramovici teaches wherein the plurality of setting data represent a plurality of divided circuits obtained by dividing one circuit as **[the set of FPGAs which form the reconfigurable hardware implements a single logic circuit, having any desired size, by partitioning the circuit's netlist into "subcircuit portions", each of which is represented by a portion of the initial netlist generally referred to as a page (column 3, lines 32-45)].**

As per claim 27, Abramovici teaches wherein the reconfigurable circuit is configured as a combinational circuit as **[the reconfigurable hardware can be made of a number of any commercially available FPGAs or via a single FPGA (column 4, lines 39-52) which are inherently formed of logic blocks operating via combinational functions, forming a combinational circuit].**

As per claim 28, Abramovici teaches an output circuit receiving an output of the reconfigurable circuit as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register**

values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)] and providing the output of the reconfigurable circuit when the reconfigurable circuit is configured a plurality of times by the setting portion as [the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)].

As per claim 29, Abramovici teaches a switching circuit switching between the input from the second path and an external input, to be an input to the reconfigurable circuit as [the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2) where the page manager directs the connecting and disconnecting of the I/O pins of the FPGA being configured (column 5, lines 63-65) including the connections to various other types of external non-FPGA hardware (column 4, lines 51-56) which inherently includes inputs available from the connected hardware].

As per claim 30, Abramovici teaches wherein the reconfigurable circuit includes a plurality of logic circuits, each capable of selectively executing a plurality of operation functions as [the reconfigurable hardware 20 is composed of a number of FPGAs

(column 4, lines 3-9 and figure 2) where FPGAs are inherently capable of execution a plurality of functions], a connecting portion allowing setting of connections among the logic circuits as [the page manager controls loading and unloading of pages form the local memory into the FPGAs and controls storage and transfer between the FPGAs (abstract)] and the setting portion sets the functions of said connections among the logic circuits as [the local memory includes dedicated areas for storing configuration information (column 4, lines 13-15) which is supplied, via the page manager, to the FPGAs (column 5, lines 3-5)].

As per claim 34, Abramovici teaches a reconfigurable circuit allowing change in function and connection relation as [a set of reconfigurable hardware including a number of field programmable gate arrays (FPGAs) (abstract)], a setting portion storing setting data representing a divided unit forming a part of a circuit and supplying the setting data to the reconfigurable circuit as [the local memory includes dedicated areas for storing configuration information (column 4, lines 13-15) which is supplied, via the page manager, to the FPGAs (column 5, lines 3-5)], a control portion controlling the setting portion such that a plurality of setting data are successively supplied to the reconfigurable circuit to configure the intended circuit as [the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10)],

wherein the reconfigurable circuit has at least one state holding circuit holding an internal state as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10)]**, said reconfigurable circuit is divided by an arrangement of said state holding circuit into a plurality of stages of reconfigurable units as **[the reconfigurable hardware 20 is composed of a number of FPGAs (column 4, lines 3-9 and figure 2) where FPGAs are inherently capable of execution a plurality of functions]**, and the control portion controls the setting portion such that when a plurality of circuits are to be configured, setting data for configuring divided units, each forming a part of the circuits on respective stages of the reconfigurable units are successively supplied along a process flow as **[the set of FPGAs which form the reconfigurable hardware implements a single logic circuit, having any desired size, by partitioning the circuit's netlist into "subcircuit portions", each of which is represented by a portion of the initial netlist generally referred to as a page (column 3, lines 32-45) supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)]**.

As per claim 35, Abramovici teaches wherein the reconfigurable circuit is divided by an arrangement of N state holding circuits into N+1 stages of reconfigurable units as

[the set of FPGAs which form the reconfigurable hardware implements a single logic circuit, having any desired size, by partitioning the circuit's netlist into "subcircuit portions", each of which is represented by a portion of the initial netlist generally referred to as a page (column 3, lines 32-45) supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)], the control portion controls the setting portion such that at one point in time, setting data of a divided unit configuring a circuit is supplied to the reconfigurable unit between the i -th state holding circuit and the $(i+1)$ -th state holding circuit as [the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs (from local memory) and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)], and controls said setting portion such that at a next time point, setting data of a next divided unit configuring said circuit is supplied to the reconfigurable unit between the $(i+1)$ th state holding circuit and the $(i+2)$ th state holding circuit in accordance with the process flow, and controls said setting portion such that setting data of a divided unit configuring a different circuit is supplied to the reconfigurable unit between the i -th state holding circuit and the $(i+1)$ -th state holding circuit as [the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs (from local memory) and stores information

regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) where each unit formed by a page of configuration information for supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)].

As per claim 36, Abramovici teaches wherein the reconfigurable circuit is divided by the arrangement of N state holding circuits into N stages of reconfigurable units as **[the set of FPGAs which form the reconfigurable hardware implements a single logic circuit, having any desired size, by partitioning the circuit's netlist into "subcircuit portions", each of which is represented by a portion of the initial netlist generally referred to as a page (column 3, lines 32-45) supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)]**, said control portion controls said setting portion such that at one time point, setting data of a divided unit configuring a circuit is supplied to the reconfigurable unit between the i-th state holding circuit and the (i+1)-th state holding circuit as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs (from local memory) and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) where each unit formed by a**

page of configuration information for supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)], and controls said setting portion such that at a next time point, setting data of a next divided unit configuring said circuit is supplied to the reconfigurable unit between the (i+1)th state holding circuit and the (i+2)th state holding circuit in accordance with the process flow, and controls said setting portion such that setting data of a divided unit configuring a different circuit is supplied to the reconfigurable unit between the i-th state holding circuit and the (i+1)-th state holding circuit as [the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs (from local memory) and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) where each unit formed by a page of configuration information for supplying the configurations successively as the appropriate configuration is needed (column 3, lines 56-67; figure 4 and the abstract)] and a path portion for providing an input from the N-th state holding portion to the first stage of reconfigurable units as [the page manager is operative to route signals between the output of one page loaded into the reconfigurable hardware to the input of the next page loaded into the reconfigurable hardware (column 5, lines 3-10)].

As per claim 37, Abramovici teaches wherein the reconfigurable unit is configured as a combinational circuit as [the reconfigurable hardware can be made

of a number of any commercially available FPGAs or via a single FPGA (column 4, lines 39-52) which are inherently formed of logic blocks operating via combinational functions, forming a combinational circuit].

As per claim 38, Abramovici teaches an output circuit receiving an output of the reconfigurable circuit as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)]** and providing the output of the reconfigurable circuit when the reconfigurable circuit is configured a plurality of times by the setting portion as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)].**

As per claim 39, Abramovici teaches an internal state holding circuit receiving an output of the reconfigurable circuit and a first path portion inputting the output signal held by said internal state holding circuit to the first stage of reconfigurable units as **[the page manager (PAGMAN 22) includes one or more first-in-first-out (FIFO) buffers for use in controlling storage and transferring inter-page signal values (i.e. storing the output of one page, to be provided as the input to another) (column 5, lines 10-21 and figure 3)].**

As per claim 40, Abramovici teaches a memory portion storing in a prescribed area an output of said reconfigurable circuit in accordance with setting data as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)]** and a second path portion transmitting the output of the circuit configured on the reconfigurable circuit, which is stored in the memory portion, as an input to a circuit configured in accordance with the next setting data as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)]**.

As per claim 41, Abramovici teaches a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit as **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2) where the page manager directs the connecting and disconnecting of the I/O pins of the FPGA being configured (column 5, lines 63-65) including the connections to various other types of**

external non-FPGA hardware (column 4, lines 51-56) which inherently includes inputs available from the connected hardware].

As per claim 42, Abramovici teaches wherein the reconfigurable unit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions as **[the reconfigurable hardware 20 is composed of a number of FPGAs (column 4, lines 3-9 and figure 2) where FPGAs are inherently capable of execution a plurality of functions]**, a connection portion allowing setting of connection relations among the logic circuits as **[the page manager (PAGMAN 22) controls the loading and unloading of pages for each of the FPGAs and stores information regarding which page is loaded at any given time, as well as a mapping of pages and their locations in the memory and is operative to route signals between loaded pages (column 5, lines 3-10) as well as controlling storage and transfer of information between the FPGAs (abstract)]** and said setting portion sets the functions and said connection relation of said logic circuits as **[the page manager controls loading and unloading of pages form the local memory into the FPGAs and controls storage and transfer between the FPGAs (abstract)]**.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 31 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici (US 6034538) in view of Mansingh (US 6745318).

As per claim 31, Abramovici teaches the processing device according to claim 30, as described above.

Abramovici does not explicitly teach wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations, however.

Mansingh teaches wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations as **[a dynamic arithmetic unit 18, including at least one configurable arithmetic unit 20 capable of performing operations from decoded instructions 24, provided by the decoder 16 (column 2, lines 38-47 and figure 1)]**.

Abramovici and Mansingh are analogous art, as they are within the same field of endeavor, namely reconfigurable processing.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use the configurable arithmetic logic unit of Mansingh in the reconfigurable circuit of Abramovici.

The motivation for doing so, as provided by Mansingh, would have been **[to decrease the size of the combined arithmetic logic units' integrated circuit footprint by providing a single reconfigurable arithmetic logic unit, thus reducing costs (column 1, lines 48-54)]**.

As per claim 43, Abramovici teaches the processing device according to claim 42, as described above.

Abramovici does not explicitly teach wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations, however.

Mansingh teaches wherein the logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations as **[a dynamic arithmetic unit 18, including at least one configurable arithmetic unit 20 capable of performing operations from decoded instructions 24, provided by the decoder 16 (column 2, lines 38-47 and figure 1)]**.

Abramovici and Mansingh are analogous art, as they are within the same field of endeavor, namely reconfigurable processing.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use the configurable arithmetic logic unit of Mansingh in the reconfigurable circuit of Abramovici.

The motivation for doing so, as provided by Mansingh, would have been **[to decrease the size of the combined arithmetic logic units' integrated circuit**

footprint by providing a single reconfigurable arithmetic logic unit, thus reducing costs (column 1, lines 48-54)].

Conclusion

11. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 1-22, 32 and 33 have been withdrawn, claims 23-31 and 34-43 are rejected.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Vorbach (US 20060248317) – teaches a reconfigurable circuit which can be divided dynamically to perform given operations.

14. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

15. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Giroux whose telephone number is 571-272-9769. The examiner can normally be reached on Monday through Friday, 8:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

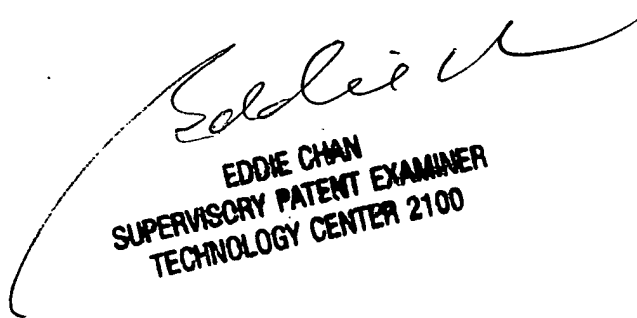
Application/Control Number:
10/573,970
Art Unit: 2183

Page 21

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1-5-08

George Giroux
Examiner
Art Unit 2183



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100